Field-driven test contacting solution

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In today's semiconductor industry, test technology is improving and moving forward dramatically. With the continuous increase of market needs and complexities, the problem of integrated circuit (IC) testing has become much more challenging and needs an economic solution with reliable and sustainable performance. Various analyses (internal and in conjunction with end users as well as [1]) on test field challenges and customer "pains" revealed that a solution addressing current issues must be designed.

The main objectives of any production test are to be able to rely on test data and not spend time on repetitive tests, and to avoid test failures. To determine the contact resistance of a rigid pin, we need to understand the internal mechanics of the pin assembly as well as the resistance network that allows the flow of current. A new rigid contactor called Zigma (**Figure 1**), which utilizes short wipe stroke (SWS) technology, enables various plated devices to test millions of insertions. This new design addresses the false failure

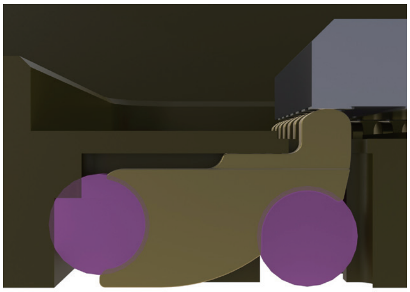

Figure 1: Zigma pin with front and back elastomer.

phenomenon in final production test by virtue of its having increased co-planarity between the front and back elastomer configuration (**Figure 1**). When assembled with an increased pre-tension, the bottom elastomer is compressed to the operating height that will accommodate standard pad height variations on the target PCB. Similarly, on the top side, the device compresses the top elastomer to its operating height to accommodate the device's co-planarity. In this compressed state, the tips of the pin penetrate through the layer of oxides of tin on the device under test (DUT) allowing current to flow through the advanced profile. Because the device has wide co-planarity, not all of the pins available in the test industry market today are compressed to exactly the operating height. If the plungers are not compressed to the same operating height, the engagement to the device pads will be different, which in turn results in a large variation in contact resistance. This enhanced feature allows production workers to test and verify without multiple repeat testing.

It is also the contactor designer's duty to ensure that the lifetime of the DUT boards is not compromised, which is one of the most discussed issues in the test industry. The new technology on the contactor surface with its advanced contact finish (ACF) (**Figure 2**) and motion dynamics ensures that the DUT board, even after millions of cycles of insertions, is not degraded.

Development objectives

There are several factors that need to be taken into account in highlighting product configuration for various plated device applications: first is the contact pin profile itself. Different device platings such as matte tin or NiPd/NiPdAu may require different contact profiles and motion dynamics. For

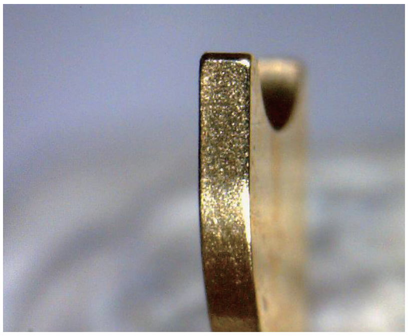

Figure 2: Zigma pin with ACF-advanced contact finish.

matte tin, the contact pin needs to break through the oxides, maintain an effective wipe action, and provide good contact resistance readings.

A second factor is the contact force. The amount of contact force needs to be compatible with the type of plating. For example, the force required for matte tin is different from that required for NiPd-plated devices. Because of the greater hardness of NiPd and prolonged plunger force, the contact tip wears prematurely. Zigma does not use its housing body as a tail end stopper. Instead, the rear elastomer is used as the tail stopper, which helps to dissipate the pressure that builds up at the contact tip and DUT board. This scheme increases the life span of the contact pin.

A third factor is the surface roughness—a key parameter. Contact pins that have a rough surface will tend to fill up with solder material when used with tin-plated devices. A smoother surface will tend to keep the contact tip clean with minimal tin migration. Having a smoother, softer gold finish on the contact will also reduce chafing when in contact with the gold plating of the load board.

Packaging considerations

Packaging has a number of influences on test methods, one of which is the issue of sawn vs. punched packages for high-frequency devices: one type with burr-free smooth edges; the other with "ragged" edges. Because of tolerance factors on the alignment pocket opening and the DUT, the sharp burrs from the sawn packages hit the contact tip of the pin and get dislodged from the DUT when exposed to vibrations. This situation causes severe damage to the contact tip up. Additionally, the burr particle that falls on the DUT board has a "sand paper" effect leaving the board severely damaged. With the help of SWS technology, the contact tip is placed further inside of the device pad edge, thereby avoiding the sharp burrs that occur with sawn packages. The result is less contamination formation and debris collection and increased pin contact life.

Trends in packaging such as dimple pads/wettable flank (**Figure 3**), corner chamfer pads (**Figure 4**), and short pads are becoming increasingly popular. It is therefore becoming highly challenging to test with the rigid contact solutions currently available as the pad length needed to make a good scrub exceeds the wipe length, thereby resulting in contact failure. A potential test challenge now facing the industry is the use of devices with corner chamfer pads as shown in **Figure 4**. For such pads, the available pad length is 0.2mm maximum, where the scrubbing should take place without smearing the pads to the die, which will result in neither a test failure nor a quality rejection. The SWS technology addresses this issue by providing a good wipe length of ≤0.10mm that will land well inside the very short pads of the devices.

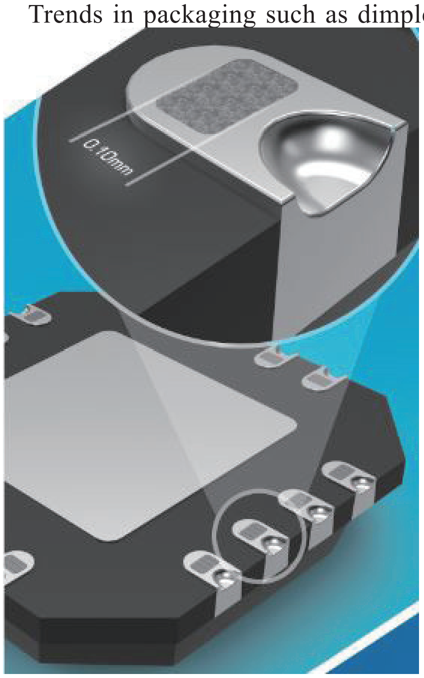

Figure 3: Wettable flank/dimple pad device.

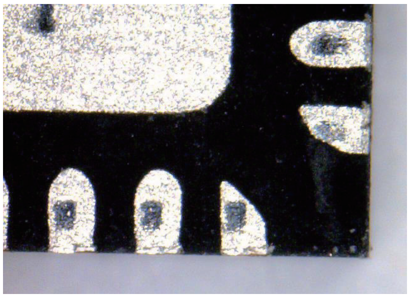

Figure 4: Corner chamfer pads.

Summary

A new contacting solution is designed to meet several of the most challenging issues facing semiconductor test. The new design provides sustainable performance in terms of less cleaning, reduced cost-of-test, longer MTBA/MTBR, higher operational equipment efficiency (OEE), and high first-pass yield.

References

1. "The future is the interconnect: IITC," online, cited Aug. 10, 2012; http://www.monolithic3d.com/2/category/tsv/1.html

Biography

Shamal Mundiyath received his MSc in Engineering and Manufacturing Management from Coventry U. MSRSAS and is Head of the Department-Engineering at JF Microtechnology SDN BHD; email shamal.mundi@jftech.com.my